

Application No.: 10/005,627

Docket No.: JCLA6897

In The Claims:

Claim 1. (currently amended) A motherboard with reduced power consumption, comprising:

a memory module slot for receiving a memory module therein;

a DDR (Double data rate) termination array, coupled between the memory module slot and a voltage source, comprising a plurality of termination resistors connected to the voltage source and a plurality of switches between the plurality of termination resistors and the memory module slot, wherein the plurality of switches controlling connections between the memory module slot and the termination resistors are controlled according to a control signal; and

a controller chip set, coupled to the memory module slot and the DDR termination array, providing the control signal, wherein when the motherboard enters a power saving mode, or before the memory module is inserted into the memory module slot, the control signal opens the plurality of switches to cut ~~[[cuts]]~~ off the coupling connections ~~between the termination resistors~~ memory module slot and the voltage source; and wherein in connection, the plurality of termination resistors are coupled to the memory module in the memory module slot through the plurality of switches.

2. (original) The motherboard according to claim 1, wherein the control signal includes a clock enable signal.

3. (original) The motherboard according to claim 1, wherein the memory module comprises a double data rate dynamic random access memory (DDR DRAM).

4. (original) The motherboard according to claim 1, wherein the motherboard is used in a laptop computer.

5. (original) The motherboard according to claim 1, wherein the controller chip set comprises a north bridge chip.

6. (previously presented) The motherboard according to claim 1, wherein the DDR termination array further comprises:

a plurality of signal terminals, coupled between the memory module slot and the plurality of switches.

7. (canceled)

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8. (currently amended) A motherboard with reduced power consumption, comprising:
a memory module slot for receiving a memory module;
a plurality of termination resistors, coupled to the memory module slot;
a switch, coupled between the plurality of termination resistors and a voltage source,
on/off of the switch being controlled by a control signal; and
a controller chip set, coupled to the memory module slot and the switch to provide the control signal, wherein when the motherboard enters a power saving mode or when the memory module is not inserted in the memory module slot, the control signal commands the switch to cut off the connection between the termination resistors and the voltage source; and wherein in connection, the plurality of termination resistors are coupled to the memory module in the memory module slot via the switch.
9. (original) The motherboard according to claim 8, wherein the control signal comprises a clock enable signal.
10. (original) The motherboard according to claim 8, wherein the memory module comprises a double data rate dynamic random access memory (DDR DRAM).
11. (original) The motherboard according to claim 8, wherein the motherboard is used in a laptop computer.
12. (original) The motherboard according to claim 8, wherein the controller chip set comprises a north bridge chip.
13. (previously presented) An operation method of a motherboard with reduced power consumption, wherein the motherboard comprises a memory module slot for receiving a memory module and a plurality of termination resistors, the termination resistors and a voltage source form an operation circuit, the operation method comprising:
using a control signal to cut off a connection between the memory module and the operation circuit when the motherboard enters a power saving mode or when the memory module slot is not inserted with the memory module; and

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using the control signal to establish the connection between the memory module slot and the operation circuit when the motherboard enters a normal operation mode and when the memory module slot is inserted with the memory module.

14. (original) The operation method according to claim 13, wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the memory module slot.

15. (original) The operation method according to claim 13, wherein the cutting off step comprises a step of cutting off connections between the termination resistors and the voltage source.

16. (previously presented) The operation method according to claim 13, wherein the control signal is a clock enable signal provided by a laptop computer.